IN THE CLAIMS

The status of Claims 1-29 is as follows.

1. (Previously Presented) An apparatus for designing a memory for use in an embedded processing system comprising:

a simulation controller capable of simulating execution of a program to be executed by said embedded processing system;

a memory access monitor capable of monitoring memory accesses to a simulated memory space during said simulated execution of said program, wherein said memory access monitor is capable of generating memory usage statistical data associated with said monitored memory accesses, and wherein said memory accesses comprise read operations and write operations; and

a memory optimization controller capable of comparing said memory usage statistical data and one or more design criteria associated with said embedded processing system and, in response to said comparison, determining at least one memory configuration capable of satisfying said one or more design criteria.

2. (Previously Presented) The apparatus as set forth in Claim 1 wherein said at least one memory configuration is determined from a set of memory types, said set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM).

3. (Original) The apparatus as set forth in Claim 2 wherein said at least one memory configuration comprises a first memory type and a first memory size associated with said first memory type.

4. (Original) The apparatus as set forth in Claim 3 wherein said at least one memory configuration further comprises a second memory type and a second memory size associated with said second memory type.

5. (Previously Presented) The apparatus as set forth in Claim 1 wherein said simulation controller simulates execution of said program N times and wherein said memory access monitor monitors said memory accesses during said N simulated executions of said program and generates said memory usage statistical data based on said N simulated executions of said program.

6. (Previously Presented) The apparatus as set forth in Claim 1 wherein said memory optimization controller is further capable of determining at least one figure of merit associated with said at least one memory configuration, wherein said at least one figure of merit indicates a degree to which said at least one memory configuration satisfies said one or more design criteria.

7. (Previously Presented) The apparatus as set forth in Claim 1 further comprising a code optimization controller capable of modifying said program in response to said comparison of said memory usage statistical data and said one or more design criteria to thereby enable said embedded processing system to execute said program according to said one or more design criteria.

8. (Previously Presented) A method of designing an embedded processing system, the method comprising the steps of:

simulating execution of a program to be executed by the embedded processing system;

monitoring memory accesses to a simulated memory space during the simulated execution of the program, wherein said memory accesses comprise read operations and write operations;

generating memory usage statistical data associated with the monitored memory accesses;

comparing the memory usage statistical data and one or more design criteria associated with the embedded processing system; and

in response to the comparison, determining at least one memory configuration capable of satisfying the one or more design criteria.

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9. (Previously Presented) The method as set forth in Claim 8 wherein the at least one memory configuration is determined from a set of memory types, the set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM).

10. (Original) The method as set forth in Claim 9 wherein the at least one memory configuration comprises a first memory type and a first memory size associated with the first memory type.

11. (Original) The method as set forth in Claim 10 wherein the at least one memory configuration further comprises a second memory type and a second memory size associated with the second memory type.

12. (Previously Presented) The method as set forth in Claim 8 wherein the step of simulating execution of the program comprises the sub-steps of simulating execution of the program N times, wherein the step of monitoring the memory accesses comprises the sub-steps of monitoring the memory accesses during the N simulated executions of the program, and wherein the step of generating the memory usage statistical data is based on the N simulated executions of the program.

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13. (Previously Presented) The method as set forth in Claim 8 further comprising the step of determining at least one figure of merit associated with the at least one memory configuration, wherein the at least one figure of merit indicates a degree to which the at least one memory configuration satisfies the one or more design criteria.

14. (Previously Presented) The method as set forth in Claim 8 further comprising the step of modifying the program in response to the comparison of the memory usage statistical data and the one or more design criteria to thereby enable the embedded processing system to execute the program according to the one or more design criteria.

15. (Original) An embedded processing system designed according to the method as set forth in Claim 8.

16. (Original) An embedded processing system designed according to the method as set forth in Claim 9.

17. (Original) An embedded processing system designed according to the method as set forth in Claim 10.

18. (Original) An embedded processing system designed according to the method as set forth in Claim 11.

19. (Original) An embedded processing system designed according to the method as set forth in Claim 12.

20. (Original) An embedded processing system designed according to the method as set forth in Claim 13.

21. (Original) An embedded processing system designed according to the method as set forth in Claim 14.

22. (Previously Presented) For use in a processing system, a computer-readable storage medium containing computer-executable instructions for designing a memory for use in an embedded processing system, the computer-executable instructions comprising the steps of:

simulating execution of a program to be executed by the embedded processing system;

monitoring memory accesses to a simulated memory space during the simulated execution of the program, wherein said memory accesses comprise read operations and write operations;

generating memory usage statistical data associated with the monitored memory accesses;

comparing the memory usage statistical data and one or more design criteria associated with the embedded processing system; and

in response to the comparison, determining at least one memory configuration capable of satisfying the one or more design criteria.

23. (Previously Presented) The computer-readable storage medium as set forth in Claim 22 wherein the at least one memory configuration is determined from a set of memory types, the set of memory types comprising at least two of static random access memory (SRAM), dynamic random access memory (DRAM), read-only memory (ROM), flash RAM (FLASH), and electronically erasable programmable read-only memory (EEPROM).

24. (Original) The computer-readable storage medium as set forth in Claim 23 wherein the at least one memory configuration comprises a first memory type and a first memory size associated with the first memory type.

25. (Original) The computer-readable storage medium as set forth in Claim 24 wherein the at least one memory configuration further comprises a second memory type and a second memory size associated with the second memory type.

26. (Previously Presented) The computer-readable storage medium as set forth in Claim 22 wherein the step of simulating execution of the program comprises the sub-steps of simulating execution of the program N times, wherein the step of monitoring the memory accesses comprises the sub-steps of monitoring the memory accesses during the N simulated executions of the program, and wherein the step of generating the memory usage statistical data is based on the N simulated executions of the program.

27. (Previously Presented) The computer-readable storage medium as set forth in Claim 22 further comprising the step of determining at least one figure of merit associated with the at least one memory configuration, wherein the at least one figure of merit indicates a degree to which the at least one memory configuration satisfies the one or more design criteria.

28. (Previously Presented) The computer-readable storage medium as set forth in Claim 22 further comprising the step of modifying the program in response to the comparison of the memory usage statistical data and the one or more design criteria to thereby enable the embedded processing system to execute the program according to the one or more design criteria.

29. (Previously Presented) The apparatus of Claim 1, wherein the memory usage statistical data comprises at least one of:

one or more first histograms based on variable names contained in the program to be executed by the embedded processing system; and

one or more second histograms based on memory locations accessed by the program to be executed by the embedded processing system.